XILINX®

Chapter 9

Package Marking

The Virtex®-5QV FPGA package is marked as shown in Figure 9-1 and explained in Table 9-1.

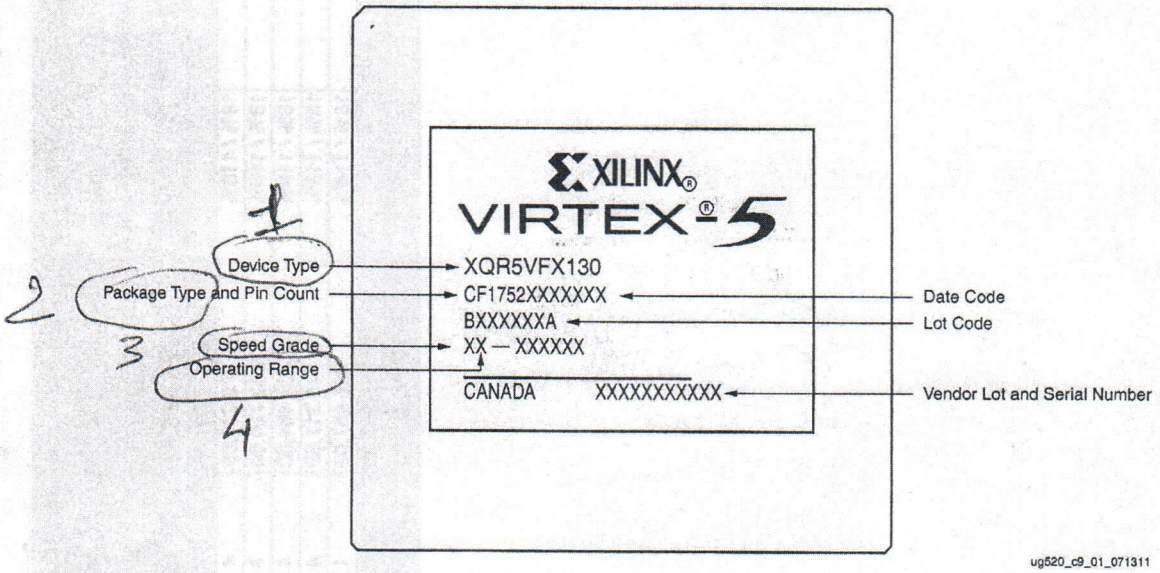

Figure 9-1: **Virtex-5QV FPGA Device Package Marking**

Table 9-1: **Device Marking Definition**

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Virtex-5 family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package type and pin count, circuit design revision, the location code for the wafer fab, the geometry code, and date code.
3rd Line	Eight alphanumeric characters for assembly, lot, and step information. The last digit is usually an *A* or an *M* if a stepping version does not exist.

Virtex Device/Package Combinations and Maximum I/O

Table 3: **Virtex Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)**

Package	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	98	98							
PQ240	166	166	166	166	166				
HQ240						166	166	166	
BG256	180	180	180	180					
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG676						404	444	444	
FG680							512	512	512

Virtex Ordering Information

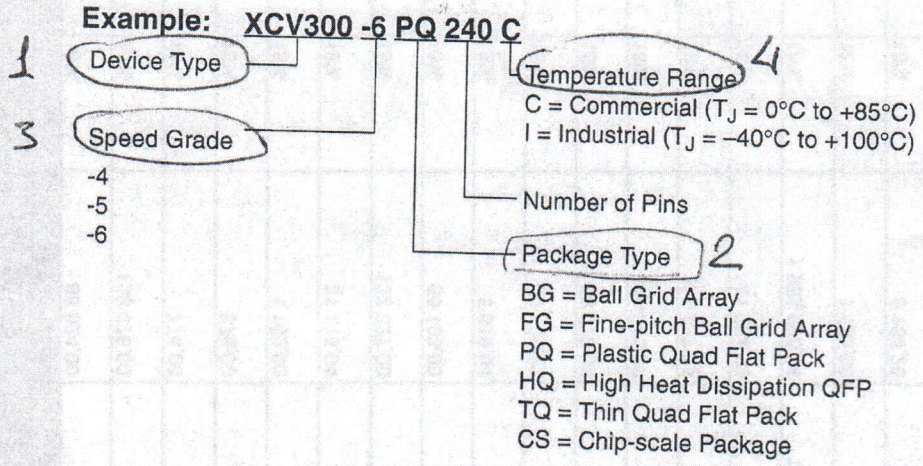

Figure 1: **Virtex Ordering Information**